4/ IDS
E. Willis
8-21-02

219.40780X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): B. CHANDRAN ET AL.

Serial No.: New Application

Filed: December 21, 2001

For: SEMICONDUCTOR PACKAGE WITH LOW RESISTANCE PACKAGE-TO-DIE INTERCONNECT SCHEME FOR REDUCED DIE STRESSES

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 & §1.98

Assistant Commissioner of Patents
Washington, D.C. 20231

December 21, 2001

Sir:

In the matter of the above-identified application, Applicants are submitting herewith copies of the documents listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This Information Disclosure Statement is being submitted concurrently with the filing of the above-identified application.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (219.40780X00) and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP

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